
In-system Programming of Cascaded AT17C/LV020 and Lower-density Devices in FPGA Applications



Introduction

Atmel's AT17 and AT17A series EEPROMs are in-system (re)-programmable for many FPGA applications. The following page introduces methods to cascade two or more AT17C/LV EEPROMs in Atmel, Xilinx and Altera FPGA applications.

Description

The in-system programming (ISP) circuit of two AT17C/LV020s in cascaded configuration is shown in Figure 1 on page 2.

The NMOS are used as switches to enable the data line. In programming mode /SER_EN is low. When the external switch is turned off, the first NMOS will be on (Gate is high), and the second NMOS will be off (Gate is low). In this case, the first EEPROM will be selected for writing data. When the external switch is turned on, the first NMOS will be off (Gate is high), and the second NMOS will be on (Gate is low). In that case, the second EEPROM will be selected for writing data. When programming the second EEPROM with data it is required to turn the external switch manually.

In the configuration mode /SER_EN is high, both NMOS are turned on, and the data line is connected. Data reading depends on the control signals from the FPGA to the /CE pin and the *RESET/OE pins of the EEPROMs.

Atmel's AT17 series EEPROM will not be programmed with floating data because it requires the device address data to enable writing data into the memory. Therefore, the device #1 in Figure 1 will not be programmed with floating data when the device #2 is accepting data. The devices #1 and #2 will not start configuration while the device #2 is programming with data because the FPGA will be held in reset while the /SER_EN line from the ISP connector is active low.

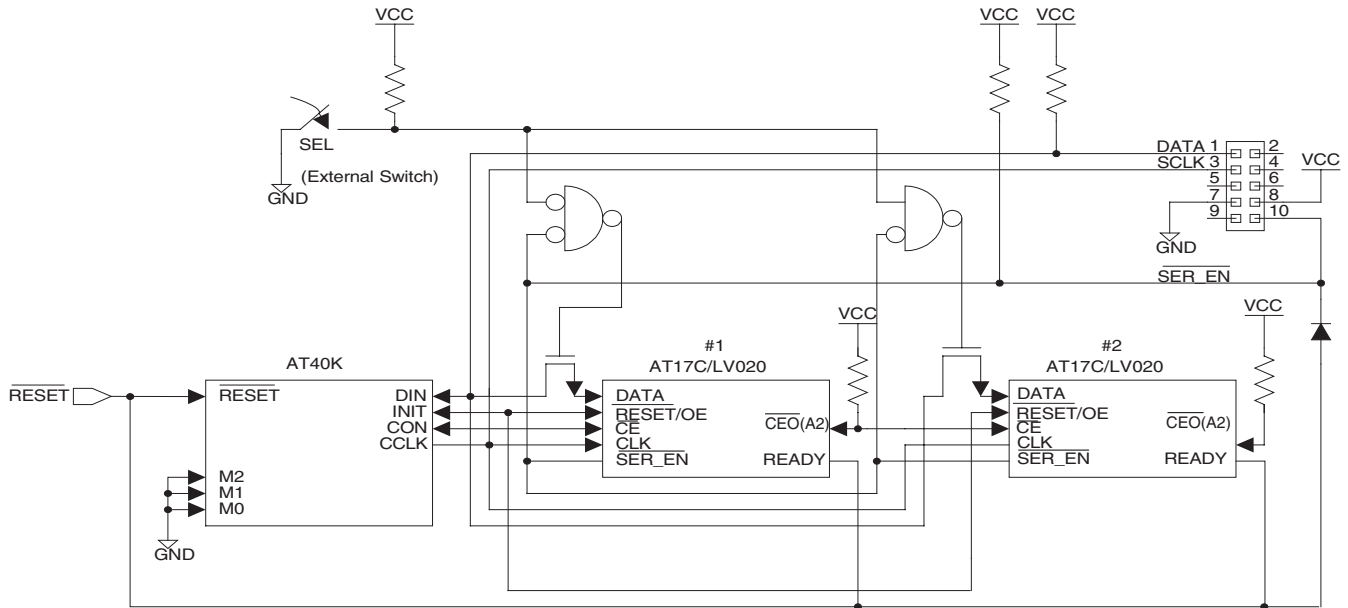
AT17 Series Configuration EEPROM Memory

Application Note

Rev. 2292A-04/01



Figure 1. ISP of 2 Casacaded AT17C/LV020s in AT40K FPGA Application



- Notes:
1. VCC = 5.5V Pull-up resistor = 4.7 k Ω
 2. VCC = 3.3V Pull-up resistor = 2.2 k Ω
 3. SEL = Close Device#2 Programmed with data
 4. SEL = Open Device#1 Programmed with data

For most configurators (128/256/512/010), a simple cascaded configurator application involving two EEPROMs, the A2 input can be used as an addressing pin (set to logic level "0" for one EEPROM and logic level "1" for the other EEPROM). The programming utility modifies the A2 bit sent in the bitstream message to target one of the two EEPROMs. Internally, the AT17C/LV020 is constructed with two AT17C/LV010s as shown in Figure 2. The /CEO (A2) pin of the first AT17C/LV010 has an internal pull down and is connected to the /CE pin of the second AT17C/LV010. Therefore the A2 pin of the second device must be pulled up to Vcc. In this case, cascading two AT17C/LV020 is just like cascading four AT17C/LV010s. Some external logic is required to switch between the devices for programming. Figure 3 on page 3 shows the equivalent circuit for a Xilinx 4000 FPGA.

Figure 2. Internal Construction of AT17C/LV020 EEPROM

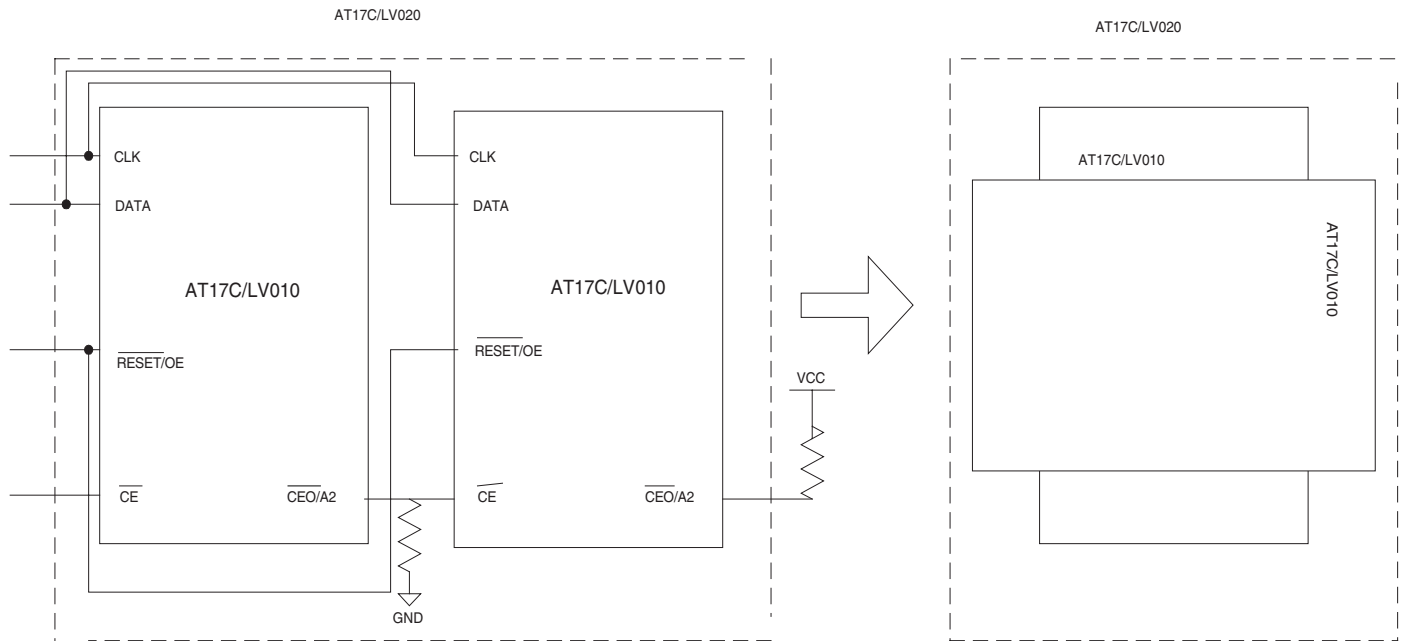
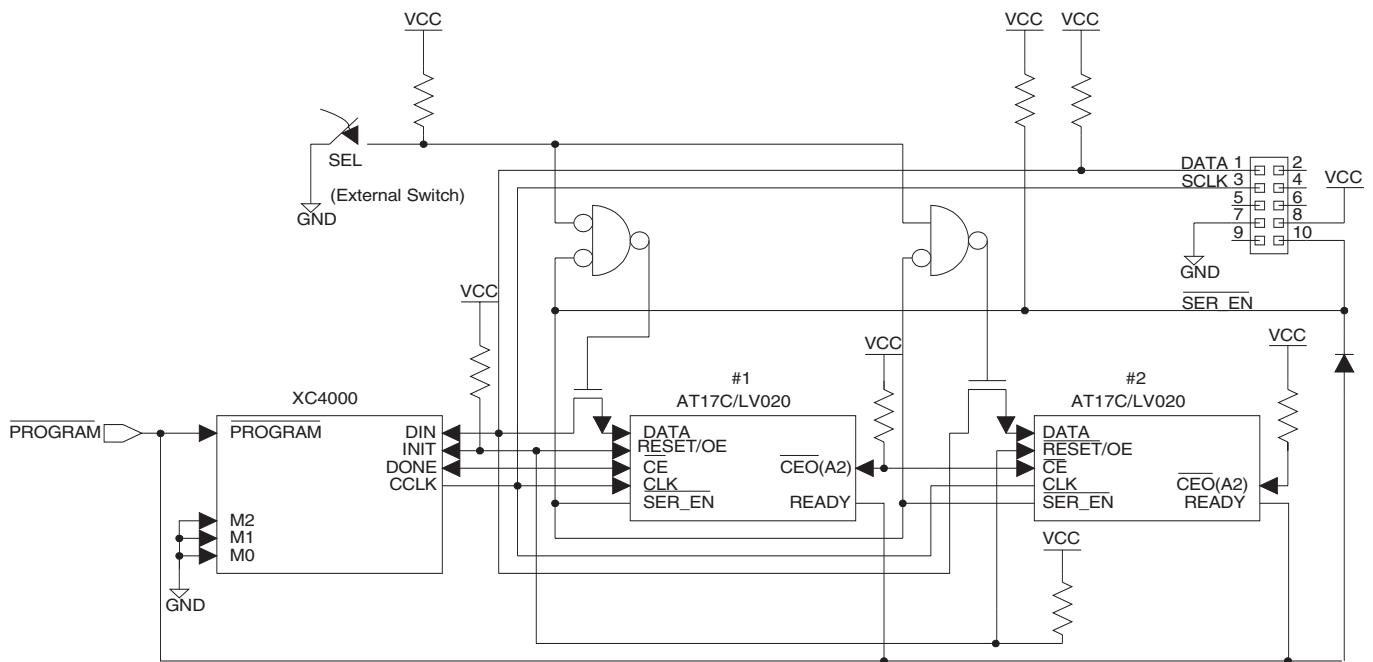


Figure 3. ISP of 2 Cascaded AT17C/LV020s in Xilinx/OR3 FPGA Application

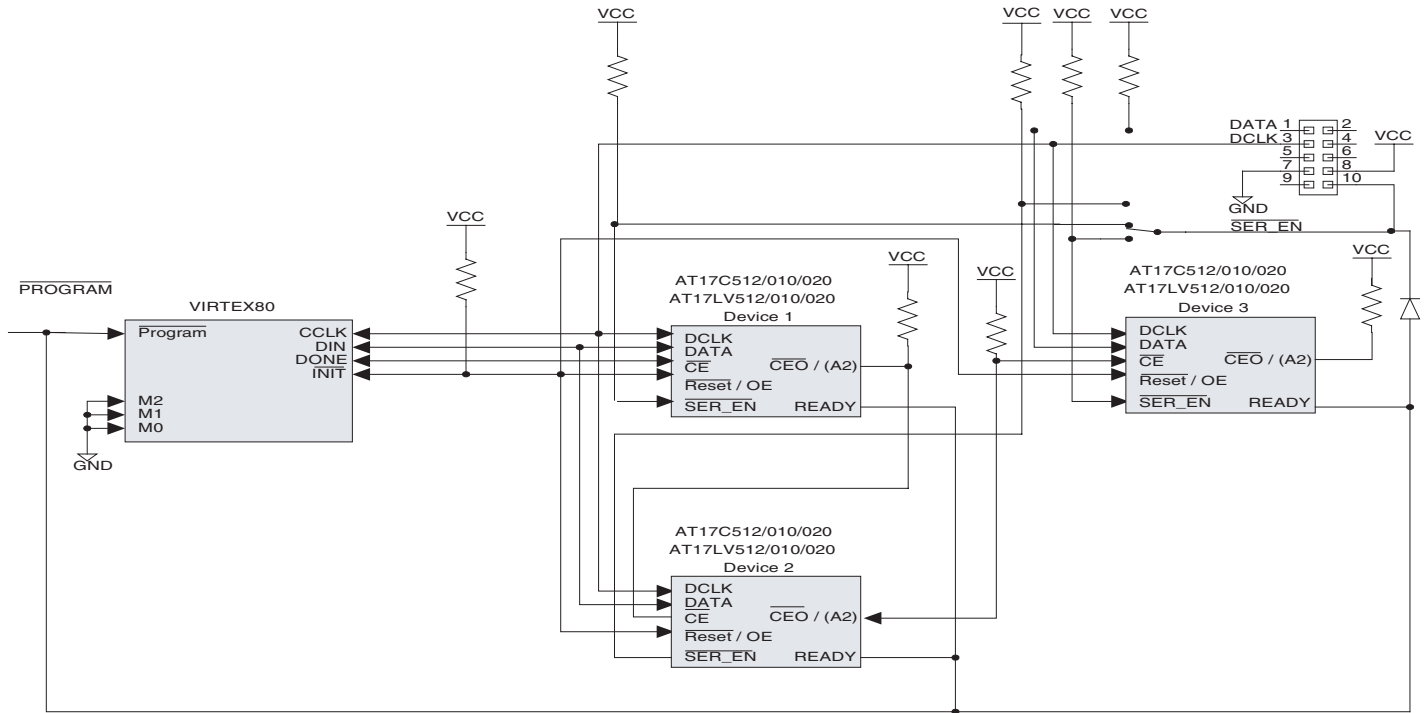


- Notes:
1. VCC = 5.5V Pull-up resistor = 4.7 k Ω
 2. VCC = 3.3V Pull-up resistor = 2.2 k Ω
 3. SEL = Close Device#2 Programmed with data
 4. SEL = Open Device#1 Programmed with data

Figure 4 displays an alternative way to cascade more than two AT17C/LV020s EEPROMs in Xilinx and Virtex FPGA Applications. This method utilizes the /SER_EN line as a switch to select which EEPROM is being programmed, since the /SER_EN must be low for data to be programmed to the device. These circuits may also be implemented using a Micro or PLD to generate the control. This would require implementing a customized download program and ISP cable to provide additional control to the circuit.

Currently the CPS software will only program the device when the user confirms the second part is ready the hardware would have to somehow recognize this event.

Figure 4. ISP of 3xAT17LV020s in Cascaded Configuration of Xilinx FPGA Application



- Notes:
1. 4.7 kΩ resistors used unless otherwise specified
 2. Use of READY pin is optional
 3. Reset polarity must be set active low
 4. RC filter recommended for input to nCONFIG to delay configuration until V_{CC} is stable



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